REMARKS

In the Final Office Action dated July 3, 2008, the Office maintained prior rejections of the pending Claims 1, 3, 6, 7, 12, 14-16, 32-24, 42, 46, 47, and 64-67 based on §102(b) in view of US Pub. No. 2001/0023425 to Oberman et al. because the prior Response dated March 28, 2008 was asserted as containing only a general statement. In particular, it appears that the Examiner issued a Final Office Action because the prior Response only submitted a "general statement" of patentability without substantive arguments as how the prior rejections were overcome.

Applicants respectfully submit that this was not the case, and formally request that the finality of the Office Action dated July 3, 2008 be withdrawn and that the arguments presented in the Response dated March 28, 2008 (reproduced below) now be considered on the merits.

Under MPEP§707.07(f), "an examiner must provide clear explanation of all actions taken by the examiner during a prosecution of an application," that is, "[w]here the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it." It is respectfully submitted, as further explained below, this did not happen, and accordingly, Applicants request that the finality of the Office Action dated July 3, 2008 be withdrawn per MPEP§706.07(d).

In particular, in the Response dated March 28, 2008, in response to the Notice of Non-Compliant Amendment dated February 28, 2008 with respect to the Amendment submitted on December 27, 2007, Applicants respectfully requested that the non-marked version of the claims, which was inadvertently submitted in the Response of August 2, 2007, please be disregarded, as it was submitted in error and does not correspond to the marked-up version of the claims. Accordingly, Applicants requested that only the marked-up version of claims submitted on August 2, 2007 be considered, as they are the intentionally submitted amendments, in its Response dated March 28, 2008 to address the non-compliant aspect.

Moreover, in view of the clarification, Applicants respectfully requested re-consideration of the corrected amendments from December 26, 2007, which was contained in the Response dated March 28, 2008, which was submitted as being in proper form.

Finally, in the Response dated March 28, 2008, Applicants requested allowance of the claims in view of the Claims presented therein and "the response submitted on December 26, 2007," that is, arguments presented in the Amendment dated December 26, 2007, which was placed in compliance by the Response dated March 28, 2008.

However, it appears that the Office inadvertently missed that "the response submitted on December 26, 2007" was incorporated by reference in the Response dated March 28, 2008, and thus, did not address the arguments contained therein substantively, determined the Response dated March 28, 2008 as including only a general statement, and issued the Final Office Action dated July 3, 2008 based on the misunderstanding.

As explained above, it is respectfully submitted that the Response dated March 28, 2008 is complete and that the Final Office Action dated July 3, 2008 be withdrawn so that the application may be considered on the merits based on the arguments presented in the Response dated March 28, 2008.

For the convenience of the Examiner, Claims presented in the Response dated March 28, 2008 are reproduced above.

Also for the convenience of the Examiner, arguments/remarks submitted via the Amendment dated December 26, 2007, which was incorporated by reference in the Response dated March 28, 2008, are reproduced below.

********** START OF REPRODUCTION **********

REMARKS

Claims 1, 3, 6-7, 12, 14-16, 32-34, 42, 46-47 and 64-67 are pending with Claims 1 and 32 as independent claims. The Examiner objected to Claim 12 because it is a duplicate of Claim 7. The Examiner rejects the claims under 35 USC §102(b) as being anticipated by Oberman et al. (US Pub. No. 2001/0023425).

Reconsideration of the instant application in view of the above amendments and the following remarks is respectfully requested.

Regarding the assertion that Claim 12 is a substantial duplicate of Claim 7, the Applicants respectfully disagree. Claim 12 recites among others: "a quotient logic and a selector" whereas Claim 7 recites "wherein the third logic performs the full addition operation using at least two Carry Save Adders (CSAs) each including a plurality of full adders." Furthermore, as in Claim 1, Claim 7 recites the 'third logic,' which corresponds to CSA 1, 2 (120,150) and FA (160) in Fig.1; Claim 12 recites the 'second logic,' which corresponds to a QUOTIENT LOGIC (130) and a SELECTOR (140) in Fig. 1. As can be seen, these two claims are substantially different. Accordingly, withdrawal of the rejection is respectfully requested.

Oberman provides a method and apparatus for multiplying signed scalar and vector operation. Particularly, Oberman discloses the multiplier apparatus calculating signs of multiplier and multiplicand operand according to Booth's algorithm, and outputting the result after repeatedly operating a partial product. Also, Fig. 16 of Oberman illustrates the multiplier apparatus realized by using a plurality of carry-save adders (CSA).

Claim 1 has been amended to better clarify the invention, and is directed to a signal processing apparatus for performing modular multiplication, whereas Oberman is directed to a method and apparatus for multiplying signed scalar and vector operation, and it fails to disclose any description related to modular multiplication. The Examiner's attention is drawn to the fact that just as signed multiplication and modular multiplication are different from each other, Oberman and the present invention are also different from each other.

Furthermore, the novel feature of the present invention is that a "third logic" determines carry input value "Carry-in" of a current clock from a carry value "cin" for correction of a previous clock, and a "second logic" outputs a modulus which is signed in the modular multiplication based on the carry input value "Carry-in" of a current clock and sign bit of a multiplicand. This feature is also recited in the second step of independent Claim 32. An object of the present invention is to reduce the number of gates of modular multiplier and power consumption. Oberman fails to disclose or fairly suggest the above recitations. Accordingly, the Examiner fails to establish a prima facie case of anticipation under 35 U.S.C. §102 because Oberman does not explicitly or impliedly disclose all the aspects of the claimed invention as recited in MPEP 706.02(IV).

Claims 2, 3, 6-7, 12, 14-16, 33-34, 42, 46-47 and 64-67 depend from independent Claims 1, and 32. Therefore, without conceding the patentability per se of dependent Claims 2, 3, 6-7, 12, 14-16, 33-34, 42, 46-47 and 64-67, they are believed to be patentably distinguished over Oberman, based on their respective dependency from independent Claims 1 and 32. Accordingly, reconsideration and withdrawal of the 35 U.S.C. § 102(b) rejection of Claims 1, 3, 6-7, 12, 14-16, 32-34, 42, 46-47 and 64-67 is respectfully requested.

In view of the above, it is believed that the subject matter of claims 1, 3, 6-7, 12, 14-16, 32-34, 42, 46-47 and 64-67 are not anticipated in view of the cited reference and are in condition for allowance. Thus, it is respectfully requested that the Examiner withdraw the 35 U.S.C.§102(b) rejection of Claims 1, 3, 6-7, 12, 14-16, 32-34, 42, 46-47 and 64-67 and reconsider said claims for allowance.

Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below. An early and favorable action is earnestly solicited.

**********END OF REPRODUCTION**********

To further point out the deficiencies of Oberman, Applicants note the following.

In the Action dated July 3, 2008, paragraph [0128], lines 8-16, paragraph [0130], paragraph [0143], lines 14-18, and FIGS. 16 and 19 of Oberman are cited for disclosing "a third logic for determining the carry input value Carry-in of the current clock from the carry value cin for correction of the previous clock and receiving the signed multiplicand and the signed modulus," as recited in independent Claim 1.

Independent Claim 32 similarly recites "finding a carry input value Carry-in of a current clock determined from a carry value cin for correction of a previous clock…and receiving the signed multiplicand and the signed modulus."

Applicants respectfully submit that cited sections of Oberman appear fail to disclose the above.

Paragraph [0128], lines 8-16 of Oberman recites:

> **198**A-F and a carry value **200**A-F. A set of carry-save adders (not shown) may be used within adder **64** to sum partial products **192** in redundant form. Advantageously, carry-save adders may significantly reduce the amount of time and die space required to sum partial products **192**. At the single-bit level, a carry-save adder will take three bits of the same significance and produce a sum value (having the same significance) and a carry value (having a significance one bit higher than the sum value). In contrast, the term "carry-

However, the above appears merely to disclose using a carry-save adder to sum partial products in a signed multiplication and outputting the sum value and the carry value in the carry-save adder. That is, while the sum value and carry value in Oberman may appear similar to, for example and as an illustration only, values of reference signs S and C as illustrated in FIG. 1 of the instant application, it fails to teach, for example, values corresponding to "a carry value cin for correcting a previous clock" and "a carry inout value Carry-in of a current clock, determined from a carry value cin for correction of a previous clock," as recited in independent Claim 1 and similarly recited in independent Claim 32.

Paragraph [0143], lines 14-18 of Oberman recites:

> LSB fix-up logic unit **288B**. Both carry-save adders **276A** and **276B** are configured to receive sum value **274A** and carry value **274B** from partial product array adder **64**. Each carry-save adder **276A** and **276B** is also configured to receive a rounding constant **268** from multiplexer **266**.

However, the above appears to merely disclose using two carry-save adders for processing the sum value and carry value, and fails to teach, for example, "determining the carry input value Carry-in of the current clock from the carry value cin for correction of the previous clock," as recited in independent Claim 1 and similarly recited in independent Claim 32.

Paragraph [0130] of Oberman recites:

> **[0130]** To ensure that final result **196** is correct when multiplier **50** is configured in a manner similar to the embodiment of **FIG. 14**, carry-propagate adder **204** may be configured to accept summands having a width equal to the cumulative width of all products **192A-F**. Assuming the length of each operand (multiplier and multiplicand) is n bits wide and comprises p vector components, each product **192A-F** will have a width of 2n/p. Thus to accommodate all products **192A-192F**, adder **204** may be 2n bits wide or wider. The redundant forms of each product **192-192F** (e.g., sum values **198A-F** and carry values **200A-F**) are conveyed as inputs to adder **204** (excluding the most significant product **192F**). In place of the most significant product **192F**, the final two summands remaining from the carry-save summation of products **192A-192F** are input to adder **204** as the most significant inputs. While adder **204** will output a 2n-bit wide result, only the most significant 2n/p bits comprise the final result **196**. This configuration advantageously allows adder **204** to propagate carry bits from lower order products to higher order products, thereby ensuring a proper result while still retaining the advantages associated with carry-save addition. Furthermore, the cost in die space of having a 2n-bit wide carry-propagate adder such as adder **204** may be reduced if other functions to performed by multiplier **50** also require a wide carry-propagate adder.

The above appears to discuss a carry propagate adder. However, it still fails to teach, for example, "determining the carry input value Carry-in of the current clock from the carry value cin for correction of the previous clock," as recited in independent Claim 1 and similarly recited in independent Claim 32.

Accordingly, at least due to deficiencies pointed out above, prima facie case for anticipation has not been established.

In view of the above, Applicants respectfully request withdrawal of the rejections, and allowance of the pending Claims 1, 3, 6-7, 12, 14-16, 32-34, 42, 46-47 and 64-67 is earnestly solicited. An early and favorable action is earnestly solicited.

Finally, with respect to arguments/remarks submitted via the Amendment dated December 26, 2007, which was incorporated by reference in the Response dated March 28, 2008, reproduced above, it is understood that terms used such as "the invention," "the novel feature of the present invention" and "the present invention," and comparison with respect to Oberman were presented to point out the deficiency/deficiencies of Oberman, that is, lack of prima facie case of anticipation. Accordingly, claims presented in the application are not constrained by such terms/comparisons, if any, and that the claims speak for themselves as to what features are included therein.

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